

Differential active balun circuit dynamic range analysis in CMOS

FR Gomez¹, MT De Leon², JR Hizon³

¹ New Product Development & Introduction, STMicroelectronics, Inc., Calamba City, Laguna, Philippines

¹⁻³ Microelectronics and Microprocessors Laboratory, University of the Philippines, Diliman, Quezon City, Philippines

Abstract

The paper presents a discussion on differential active balun circuit in terms of the dynamic range, designed and implemented in a 90nm complementary metal-oxide semiconductor (CMOS) technology. Dynamic range can be derived using noise analysis, and is an important design consideration as it determines the vulnerability of the circuit to unwanted signals such as noise. It is therefore critically important that the differential active balun circuit contributes as little noise as possible especially in the system level design of radio frequency (RF) applications.

Keywords: differential active balun; dynamic range; cmos; noise.

1. Introduction

A balun (balanced-unbalanced) circuit is a type of transformer that converts signals that are single-ended or unbalanced with respect to ground into signals that are differential or balanced with respect to ground. Baluns are further classified as either active or passive baluns depending on the components used. Active baluns are preferred over their passive counterparts because they can produce gain, occupy less chip area, and can operate at higher frequencies [1-2].

One of the active balun topologies is the differential active balun circuit in Fig. 1 consisting of 3 transistors namely M1 and M2 for the differential output, and M3 for the tail current, and is designed in a 90nm complementary metal-oxide semiconductor (CMOS) technology. The radio frequency (RF) input signal is applied at the input of one of the differential pair transistors and will ideally split equally between the pair with same amplitude and 180 degrees phase difference. Interestingly, this active balun topology is capable of producing gain.

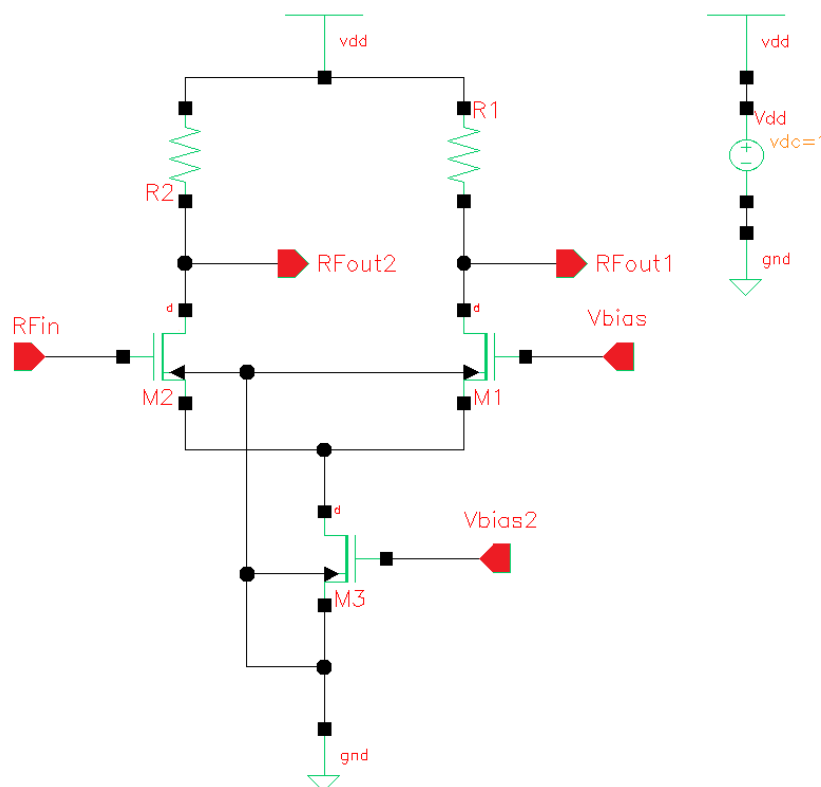


Fig 1: Differential active balun circuit schematic.

Dynamic Range Analysis

The very weak signal received by the RF circuit makes the input signal very susceptible to noise. The existence of noise is essentially due to the fact that electrical charge is not continuous but rather carried in discrete amounts equal to the electron charge [3-4]. The study of noise is important because it represents a lower limit to the size of the electrical signal that can be amplified by the RF circuit without significantly deteriorating the signal quality. Hence it is important that each block in the RF receiver contributes as little noise as possible.

Important design parameters such as dynamic range (DR) can be derived using noise analysis. Shown in Fig. 3 is the circuit model with noise sources of differential active balun transformer circuit.

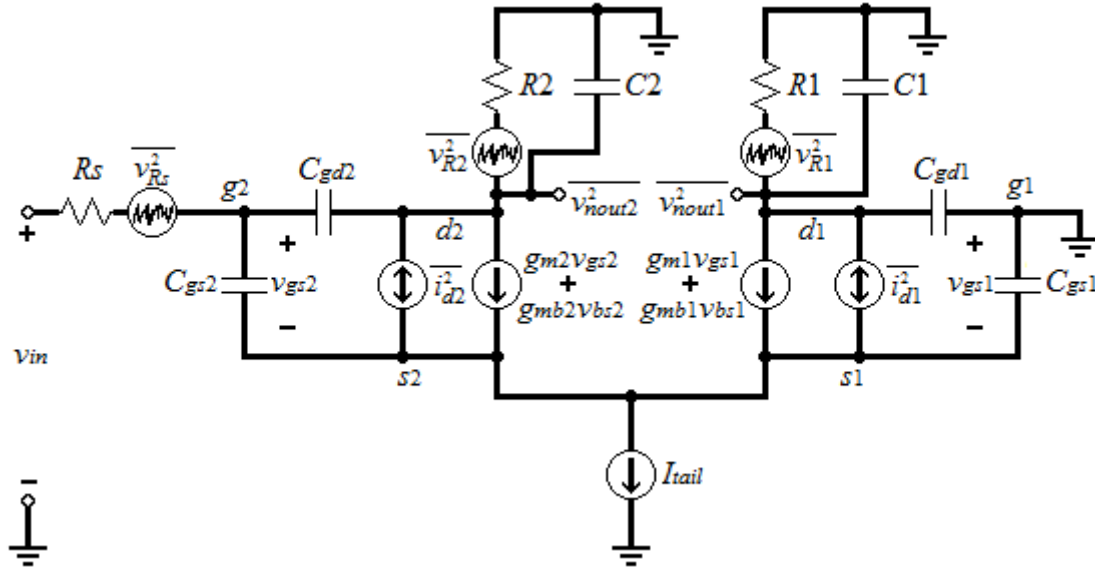


Fig 3: Differential active balun transformer model with noise generator.

Since differential active balun supplies differential input signal into a differential circuit, noise calculation for each of the two output nodes is necessary. Starting with Kirchhoff's current law (KCL) at node d2, output noise voltage and current of RFout2 are determined in the succeeding equations.

$$\overline{i_{n,out2}^2} = \overline{i_{d2,th}^2} + \overline{i_{d2,1/f}^2} + \overline{i_{R2}^2} + \frac{\overline{v_{Rs}^2} - \overline{v_{n,out2}^2}}{(1/sC_{gd2})^2} \tag{1}$$

$$\overline{v_{n,out2}^2} = \left[4k_B T \gamma (g_{m2} + g_{mb2}) \Delta f + \frac{K_f I_{D2}}{L^2 C_{ox} f_{co}} \Delta f + \frac{4k_B T}{R2} \Delta f + \frac{\overline{v_{Rs}^2} - \overline{v_{n,out2}^2}}{(1/sC_{gd2})^2} \right] \left(R2 \parallel \frac{1}{sC2} \right)^2 \tag{2}$$

At higher frequency, thermal noise of transistor dominates, hence flicker noise could be neglected. Rearranging (2), output voltage noise of RFout2 could be simplified. With source resistance (Rs) assumed to be negligible,

$$\overline{v_{n,out2}^2} = \frac{k_B T}{C2} \cdot \frac{1 + \gamma (g_{m2} + g_{mb2}) R2}{1 + \frac{1}{4} \left(\frac{C_{gd2}}{C2} \right)^2} V_{rms}^2 \tag{3}$$

If output capacitance C2 dominates rather than the inherent Cgd2, (3) could then be simplified as

$$\overline{v_{n,out2}^2} = \frac{k_B T}{C2} [1 + \gamma (g_{m2} + g_{mb2}) R2] V_{rms}^2 \tag{4}$$

From (4), increasing the resistance R2 increases the overall noise. Output capacitance C2 dictates significantly, if compared to Cgd2, on the output noise performance. Increasing the capacitance would decrease the output voltage noise but it would also decrease the circuit bandwidth or the cutoff frequency of RFout2. This design tradeoff is inevitable so one should consider the effectiveness of setting or limiting the output capacitance.

For RFout1, the output noise voltage and current could be determined starting from KCL at node d1. If the circuit is symmetric, then the noise (denoted as $i_{n,tail}$) generated in I_{tail} divides equally between M1 and M2 producing only a common-mode noise voltage at the output. If the tail current noise is negligible, that is $i_{n,tail} \ll I_{tail}$, and source resistance (R_s) assumed also to be negligible, a symmetric noise equation could be achieved. Doing KCL at node s1 (or s2),

$$\overline{i_{d1,th}^2} + \overline{i_{d1,1/f}^2} = \overline{i_{d2,th}^2} + \overline{i_{d2,1/f}^2} \tag{5}$$

Output noise voltage and current for RFout1 branch could now be expressed with KCL at node d1.

$$\overline{i_{n,out1}^2} = \overline{i_{d1,th}^2} + \overline{i_{d1,1/f}^2} + \overline{i_{R1}^2} \tag{6}$$

$$\overline{v_{n,out1}^2} = \left\{ 4k_B T \left[\gamma(g_{m1} + g_{mb1}) + \frac{1}{R1} \right] + \frac{K_f I_{D1}}{L^2 C_{ox} f_{co}} \right\} \Delta f \cdot \left[\frac{R1}{R1(sC1 + sC_{gd1}) + 1} \right]^2 \tag{7}$$

Assuming flicker noise is neglected at higher frequency,

$$\overline{v_{n,out1}^2} = \frac{k_B T}{C1 + C_{gd1}} [1 + \gamma(g_{m1} + g_{mb1})R1] \tag{8}$$

If output capacitance C1 dominates the other capacitance C_{gd1} , expression in (8) could be simplified as

$$\overline{v_{n,out1}^2} = \frac{k_B T}{C1} [1 + \gamma(g_{m1} + g_{mb1})R1] \tag{9}$$

From (9), increasing the resistance R1 increases the overall noise while increasing the load capacitance C1 decreases the circuit noise. However, increasing the capacitance C1 would also decrease the circuit bandwidth or the cutoff frequency of RFout1. This design tradeoff is inevitable so one should consider the amount of output capacitance.

Input-referred noise voltage, on the other hand, can be derived by expressing the output noise voltage with the small-signal gain. To illustrate,

$$\overline{v_{n,in}^2} = \frac{\overline{v_{n,out1}^2}}{A_{v1}^2} = \frac{\overline{v_{n,out2}^2}}{A_{v2}^2} \quad V_{rms}^2 \tag{10}$$

Using the expression for output noise voltage in (9) and (4), which is also the expression for signal-to-noise ratio (SNR), dynamic range of the circuit for the RFout1 and RFout2 side, respectively, could be determined. Dynamic range is the ratio of the maximum signal power that the circuit can tolerate without distortion to noise level of circuit. The largest signal that can be passed through the output of the circuit is limited by the supply voltage (V_{DD}). Dynamic range is expressed as

$$DR_1 = 10 \log \frac{V_{DD}^2 \cdot C1}{1 + \gamma(g_{m1} + g_{mb1})R1} + 83.828 \text{ dB} \tag{11}$$

with C1 in pF,
at room temperature

$$DR_2 = 10 \log \frac{V_{DD}^2 \cdot C2}{1 + \gamma(g_{m2} + g_{mb2})R2} + 83.828 \text{ dB} \tag{12}$$

with C2 in pF,
at room temperature

With loads for the two output nodes assumed to be equal, that is $R1 = R2$ and $C1 = C2$, the two dynamic ranges would be equal. Noise performance is an important design consideration since it determines the vulnerability of the active balun to unwanted signal like noise. Ultimately, it is critically important that the differential active balun transformer circuit contributes as little noise as possible especially in the system level design of RF applications.

Acknowledgment

The authors would like to express appreciation to the Department of Science and Technology (DOST), DOST-PCASTRD, DOST-ERDT, and Microelectronics and Microprocessors Laboratory at the Electrical and Electronics Engineering Institute of the University of the Philippines for the extensive support. Author F.R. Gomez would also like to thank the STMicroelectronics Calamba New Product Development & Introduction team and the Management Team for the extended support.

References

1. Yang HYD, Castaneda JA. Design and analysis of on-chip symmetric parallel-plate coupled-line balun for silicon RF integrated circuits," IEEE Radio Frequency Integrated Circuits Symposium 2003, pp. 527-530, June 2003.
2. Gomez FR, De Leon MT, Roque CR, Active balun circuits for WiMAX receiver front-end, TENCON 2010 – IEEE Region 10 Conference, pp. 1156-1161, November 2010.
3. Bowick C, Circuit Design RF. 1st ed., USA: Howard W. Sams & Co. In, 1982.
4. Gray PR, Hurst PJ, Lewis SH, Meyer RJ. Analysis and Design of Analog Integrated Circuits, 4th ed., New York: John Wiley & Sons, Inc, 2001.
5. Razavi B. Design of Analog CMOS Integrated Circuits, New York: McGraw-Hill, 2001.
6. Gomez FR, Hizon JR, De Leon MT. Differential active balun design for WiMAX applications, Journal of Engineering Research and Report. 2019; 4(4):1-8.
7. Gomez FR. Electronic noise and noise analysis, UP EE 220 Analog IC Design Course, February 2008.
8. Cadence Design Systems, Inc. Custom IC / analog / RF design – circuit design. [https://www.cadence.com/
content/cadence-
www/global/en_US/home/tools/
custom-ic-analog-rf-design/circuit-design.html](https://www.cadence.com/content/cadence-
www/global/en_US/home/tools/
custom-ic-analog-rf-design/circuit-design.html)